ABSTRACT

A self-locking memory circuit for a tri state data bus having multiple bit lines. The circuit includes a non-inverting buffer chip for connection to each bit line and a resistor having a predetermined electrical resistance connected across the buffer chip. The chip and resistor provide a predetermined impedance to the flow of electrical current in the self-locking circuit. The circuit changes its state when the current of the latest information on a bit line builds or lowers above or below threshold levels of the self-locking circuit.